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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RODRIGUEZ, GLENDA P	
ART UNIT	**PAPER NUMBER**
2651	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,662	SHELL ET AL.	
	Examiner	Art Unit	
	Glenda P. Rodriguez	2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, 14-18, 20-21, 23-24* is/are rejected.

7)☒ Claim(s) *12,13,19,22 and 25-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 9, 14-17 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimoda (US Patent No. 6, 122, 120).

Regarding Claim 1, Shimoda teaches an apparatus comprising:

A sampler circuit configured to generate a digital signal in response to a pre-amplified signal (Col. 3, L. 4-9. It is inherent that a digital signal before being processed it has to be digitally sampled at a certain rate (for example Nyquist frequency is a common sampling rate).); and a filter circuit configured to generate a track ID signal in response to said digital signal (Col. 4, L. 57 to Col. 5, L. 2. Shimoda teaches extracting a signal in order to produce a head position information. It is inherent that the head position information provides the information identifies the track (i.e. track ID) in which the head is currently located with respect of the disk, as specified by the Applicant in Page 5, L. 18 to Page 6, L. 17 of the Specification.), wherein said filter circuit is configured (i) as a three-tap filter (Col. 2, L. 61-67) and (ii) reject a DC offset errors in said digital signal (Col. 3, L. 1-24).

Apparatus claim 16 is drawn to the apparatus corresponding to the apparatus of using same as claimed in claim 1. Therefore apparatus claim 16 corresponds to claim 1, and is rejected for the same reasons of anticipation as used above.

Method claim 17 is drawn to the method of using the corresponding apparatus claimed in claims 1 and 16. Therefore method claim 17 corresponds to apparatus claims 1 and 16 and is rejected for the same reasons of anticipation as used above.

Regarding Claim 3, Shimoda teaches all the limitations of Claim 1. Shimoda further teach wherein the filter circuit is configured to implement multiplication coefficients of one (Pat. No. 6, 122, 120; Fig. 8, Element 66, wherein it teaches 2 delays being multiplied by a coefficient of one.).

Regarding Claim 9, Shimoda teaches all the limitations of Claim 1. Shimoda further teach a filter circuit comprising: A digital filter circuit configured to generate a filtered track ID signal (Col. 4, L. 57 to Col. 5, L. 2. Shimoda teaches extracting a signal in order to produce a head position information. It is inherent that the head position information provides the information identifies the track (i.e. track ID) in which the head is currently located with respect of the disk, as specified by the Applicant in Page 5, L. 18 to Page 6, L. 17 of the Specification.).

Regarding Claim 14, Shimoda teaches all the limitations of Claim 1. Shimoda further teaches wherein said track ID signal comprises a servo track ID signal (Col. 4, L. 57 to Col. 5, L. 2. Shimoda teaches extracting a signal in order to produce a head position information. It is inherent that the head position information is provided from the servo region of the segment and provides the information identifies the track (i.e. track ID) in which the head is currently located with respect of the disk, as specified by the Applicant in Page 5, L. 18 to Page 6, L. 17 of the Specification.).

Regarding Claim 15, Shimoda teach all the limitations of Claim 1. Shimoda further teaches wherein a servo track ID filter is configured to generate the track ID signal in response to

the digital signal (Col. 4, L. 57 to Col. 5, L. 2. Shimoda teaches extracting a signal in order to produce a head position information. It is inherent that the head position information provides the information identifies the track (i.e. track ID) in which the head is currently located with respect of the disk, as specified by the Applicant in Page 5, L. 18 to Page 6, L. 17 of the Specification.).

Regarding Claim 21, Shimoda teaches all the limitations of Claim 1. Shimoda further teach herein a filter circuit with a $1+D-2D^2$ configuration (Col. 13, L. 40. Shimoda teaches a filter circuit configuration of $g+D+gD^2$, wherein the numbers in g can be inherently 1 and –2 respectively in order to have the same configuration).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 4, 8, 10 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoda in view of Abbott et al. (US Patent No. 5, 341, 249).

Regarding Claim 4, Shimoda teaches all the limitations of Claim 1. Shimoda does not explicitly teach wherein filter circuit is immune to DC offsets and shifts from thermal asperities. However, Abbot et al. teach wherein said filter circuit is immune to DC offsets and shifts from thermal asperities (Col. 36, Lines 52-65). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimoda's invention with the

teaching of Abbott et al. in order to digitally adapt the filter to changes in the signal (Col. 4, L. 13-16 of Abbott et al.).

Regarding Claim 8, Shimoda teach all the limitations of Claim 1. Shimoda does not explicitly teach A voltage gain amplifier and a magneto-resistive head asymmetry correction circuit. However, Abbot et al. further teach wherein the sampler comprises: a voltage gain amplifier configured to receive said pre-amplified signal (Pat. No. 5, 341, 259; Col. 9, Lines 20-34 and Col. 9, Line 66 to Col. 10, Line 19); and a magneto-resistive head asymmetry correction circuit to said voltage gain amplifier (Col. 9, Line 8-34). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimoda's invention with the teaching of Abbott et al. in order to digitally adapt the filter to changes in the signal (Col. 4, L. 13-16 of Abbott et al.).

Regarding Claim 23, the combination of Shimoda and Abbott et al. teach all the limitations of Claim 8. The combination further teach wherein the sampler comprises:

> A continuous time filter coupled to said magnetic-resistive asymmetry correction circuit (Pat. No. 5, 341, 249; Col. 9, Lines 20-34 and Col. 9, Line 66 to Col. 10, Line 19);
>
> An offset cancellation circuit coupled to said continuous time filter (Pat. No. 5, 341, 249; Col. 9, Lines 20-34 and Col. 9, Line 66 to Col. 10, Line 19);
>
> And an analog to digital conversion circuit configured to generate said digital signal and coupled to said offset cancellation circuit (Pat. No. 5, 341, 249; Col. 9, Lines 20-34 and Col. 9, Line 66 to Col. 10, Line 19).

Regarding Claim 10, Shimoda teach all the limitations of Claim 1. Shimoda does not explicitly teach wherein a read channel circuit configured to generate a read data signal response to said digital data signal. However, Abbot et al. further teach a read channel circuit configured to generate a read data signal response to said digital data signal (Pat. No. 5, 341, 249; Col. 9, Line 9 to Col. 10, Line 19). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimoda's invention with the teaching of Abbott et al. in order to digitally adapt the filter to changes in the signal (Col. 4, L. 13-16 of Abbott et al.).

5. Claim 5-7, 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoda in view of Cheung et al. (US Patent No. 5, 442, 498).

Regarding Claim 5, Shimoda teaches all the limitations of Claim 1. Shimoda does not explicitly teach wherein the filter circuit is further configured to attenuate high frequencies. However, Cheung et al. teach wherein the filter circuit is further configured to attenuate high frequencies (Col. 5, Lines 30-53). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimoda's invention with the teaching of Cheung et al. in order to remove noise and harmonic that can cause PES and phase jitter (which in known to an artisan of ordinary skill in the art to be DC offset errors).

Regarding Claim 6, Shimoda teaches all the limitations of Claim 1. Shimoda does not explicitly teach wherein the filter circuit is further configured to reject low frequencies. However, Cheung et al. teach wherein the filter circuit is further configured to reject low frequencies (Col. 5, Lines 30-53). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimoda's invention with the teaching of

Cheung et al. in order to remove noise and harmonic that can cause PES and phase jitter (which in known to an artisan of ordinary skill in the art to be DC offset errors).

Regarding Claim 7, Shimoda teaches all the limitations of Claim 1. Shimoda does not explicitly teach wherein filter circuit is further configured to closely match said digital signal. Cheung et al. further teach wherein filter circuit is further configured to closely match said digital signal (Pat. No. 5, 442, 498; Col. 5, Lines 30-53). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Abbot et al.'s invention in order to remove noise and harmonic that can cause PES and phase jitter (which in known to an artisan of ordinary skill in the art to be DC offset errors).

Regarding Claim 20, Shimoda teaches all the limitations of Claim 1. Shimoda does not explicitly teach wherein is further configured to attenuate high frequencies and to reject low frequencies. However, Cheung et al. teach wherein the filter circuit is further configured to attenuate high frequencies and to reject low frequencies (Col. 5, Lines 30-53). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimoda's invention with the teaching of Cheung et al. in order to remove noise and harmonic that can cause PES and phase jitter (which in known to an artisan of ordinary skill in the art to be DC offset errors).

Regarding Claim 24, Shimoda teach all the limitations of Claim 1. Shimoda does not explicitly teach a filter circuit comprising: A track ID decoder configured to generate said track ID signal in response to said filtered track ID signal (Pat. No. 5, 442, 498; Col. 5, Lines 30-53. Cheung et al. teach that the demodulator contains a decoder which decodes the track ID signal); A position error signal (PES) filter configured to generate a filtered PES signal in response to

said digital signal and a PES demodulator configured to generate a PES signal in response to said filtered PES signal (Pat. No. 5, 442, 498; Col. 5, Lines 30-53). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimoda's invention with the teaching of Cheung et al. in order to remove noise and harmonic that can cause PES and phase jitter (which in known to an artisan of ordinary skill in the art to be DC offset errors).

6. Claims 2, 11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoda in view of Izumi et al. (US Patent No. 6, 160, 673).

Regarding Claims 2 and 18, Shimoda teaches all the limitations of Claims 1 and 16, respectively. Shimoda does not explicitly teach wherein the filter circuit is configured to implement simple multiplication integer coefficients. However, Izumi et al. teaches the filter circuit is configured to implement simple multiplication coefficients (Pat. No. 6, 160, 673; Col. 11, Line 66 to Col. 12, Line 47). It would have been obvious to modify Shimoda's invention with the teaching of Izumi et al. in order to equalize the waveform.

Regarding Claim 11, Shimoda teaches all the limitations of Claim 1. Shimoda does not explicitly teach a filter circuit that comprises: one or more delay elements configured to delay said digital signal; and a summation circuit configured to perform summation of said delayed digital signals and provide an output filtered signal. However, Izumi et al. teach a filter circuit that comprises: one or more delay elements configured to delay said digital signal; and a summation circuit configured to perform summation of said delayed digital signals and provide an output filtered signal (US Patent No. 6, 160, 673; Fig. 6, Element 63). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify

Shimoda's invention with the teaching of Izumi et al.'s invention in order to equalize the waveform.

Allowable Subject Matter

7. Claims 12, 13, 19, 22, 25, 26 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claims 12 and 19, the primary reason for allowable subject matter is the inclusion of the limitation wherein a shift left circuit configured to receive the second delayed signal and present a shifted signal.

Regarding Claim 13, the primary reason for allowable subject matter is the inclusion of the limitation wherein the filter comprises a first and second 4^{th} order delay elements.

Regarding Claim 22, the primary reason for allowable subject matter is the inclusion of the limitation wherein the track ID signal has a SNR of at least 23.58 dB.

Regarding Claim 27, the primary reason for allowable subject matter is the inclusion of the limitation wherein a three tap-filtering comprises a $1+D^4-2D^8$ filtering.

Response to Arguments

Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection due to the newly amended claims received on 6/25/2004.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (703) 305-8411. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (703) 305-4040. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gpr
November 9, 2004.

ANDREW L. SNIEZEK
PRIMARY EXAMINER